REMARKS/ARGUMENTS

Rejections 35 U.S.C. 102

Claims 1-3, 5-7 and 10-12 are rejected under 35 U.S.C. 102(b) as being allegedly anticipated by Larsen et al, (US Pat No. 5,115,500) (hereinafter Larsen). Applicants respectfully traverse in view of the following.

Independent Claim 1 recites a limitation whereby a plurality of possible meanings are associated with the instruction, as claimed. Accordingly, one instruction may have multiple meanings. Moreover, independent Claim 1 recites a limitation whereby a portion of the corresponding address is concatenated to the instruction to form an extended instruction, as claimed. Furthermore, the extended instruction is executed, as claimed.

In contrast, Larsen discloses that Figure 2 shows an example of the instruction store with partitioning illustrated for accommodating two types of different, incompatible format machine language instructions (see Larsen, col. 5, lines 41-44). Accordingly, the same instruction can be executed by two different types of incompatible format machines. Applicants respectfully submit that an instruction executable on two different types of incompatible format machines differs from an instruction with a plurality of meanings, as claimed. For example, an instruction with a plurality of meanings is operable to produce a plurality of

results on one machine whereas an instruction executable on two different types of incompatible format machines produces the same result when it is executed on each machine. Accordingly, Larsen fails to teach or suggest a plurality of possible meanings associated with the instruction, as claimed.

Moreover, Larsen discloses that the Instruction Decode Selection Register (IDSR) retains the instruction address or some portion of the instruction residing in Instruction Decode Register (IDR) (see Larsen, col. 5, lines 54-56). Larsen further discloses that the content of IDSR and IDR are taken to Instruction Decode Memory (IDM) where specific portions of the undecoded instruction in IDR may be needed, and where the IDSR identifies the address from where the instruction is fetched (see Larsen, col. 6, lines 3-15). Larsen also discloses that address resolution logic is used to access the appropriate bit fields from the IDR (see Larsen, col. 6, lines 17-20). The effect of using the fetched-from address is to permit instructions in different regions to be decoded utilizing different rules (see Larsen, col. 6, lines 25-30).

Larsen fails to explicitly teach or suggest concatenating a portion of an address to the instruction because Larsen discloses using IDSR and IDR along with the address resolution logic in order to allow an instruction in different regions (e.g., different machines) to decode using different rules (e.g., appropriate rule for a particular machine format). Therefore, Larsen fails to

explicitly teach or suggest concatenating a portion of the corresponding address to the instruction to form an extended instruction, as claimed.

Furthermore, since Larsen fails to teach or suggest forming an extended instruction, Larsen could not have taught or suggested executing the extended instruction, as claimed. *Assuming arguendo* that Larsen teaches forming an extended instruction, Larsen still fails to teach or suggest that the portion of the corresponding address determines a meaning for the extended instruction from the possible meanings, as claimed, because as discussed above Larsen fails to teach or suggest an instruction with a plurality of possible meanings, as claimed.

Accordingly, Larsen fails to teach or suggest the recited limitations of Claim 1. As such, Larsen fails to anticipate independent Claim 1, under 35 U.S.C. 102(b). Independent Claims 5 and 10 recite limitations similar to that of independent Claim 1 and are patentable for similar reasons. Dependent claims are patentable by virtue of their dependency. As such, allowance of Claims 1-3, 5-7 and 10-12 is earnestly solicited.

Rejections 35 U.S.C. 103

Claims 4, 8-9 and 13-14 are rejected under 35 U.S.C. 103(a) as being allegedly unpatentable over Larsen. Applicants respectfully traverse in view of the following.

As per Claims 4, 8 and 13, the rejection admits that Larsen fails to teach that the plurality of possible meanings include an integer type of instruction and a floating point type of instruction, as claimed. The rejection takes Official Notice that integer type and floating point type instructions are well known and required by many programs and are present in the vast majority of instructions, and therefore are included in machine languages and capable of being executed by processors. The Applicants respectfully disagree because while the use of integer type and floating point instructions may be well known abstractly, what is at issue is the use of the integer type and floating point instructions in the claimed fashion which is not known. Accordingly, Applicants respectfully request the Examiner to produce cited art to substantiate the contention that integer and floating point instructions are known in the claimed fashion, or to withdraw this rejection.

Applicants respectfully remind the Examiner that it is never appropriate to rely solely on common knowledge in the art without evidentiary support in the record as the principal evidence upon which a rejection was based and that the Examiner must point to some concrete evidence in the record in support of these findings to satisfy the substantial evidence test (see MPEP 2144.03(c)). If the Examiner is relying on personal knowledge to support the finding of what is known in the art, the examiner must provide an affidavit or declaration setting

forth specific factual statements and explanation to support the finding (see 37 CFR 1.104(d)(2) and see MPEP 2100-144).

Accordingly, Claims 4, 8 and 13 are patentable over Larsen by virtue of their dependency and are further patentable in view of the Official Notice as discussed above. As such, allowance of Claims 4, 8 and 13 is earnestly solicited.

As per Claims 9 and 14, the rejection admits that Larsen fails to teach that generating the instruction and the storing the instruction are performed by a compiler, as claimed. The rejection takes Official Notice that compilers are used to generate and store instructions in memory, allowing programmers to write code in high level languages and allowing the compiler to convert and prepare the code for execution by processor. Applicants respectfully disagree for reasons similar to that of Claims 4, 8 and 13, as discussed above. Moreover, Applicants respectfully assert that methods other than a compiler may be used to generate and store instructions in memory. For example, an extensible markup language (XML) may be used to generate and store instructions in a memory without using a compiler. Also, interpreters may be used which do not use compilers. As such, the Official Notice taken by the rejection is misplaced. As such, allowance of Claims 9 and 14 is earnestly solicited.

For the above reasons, the Applicants request reconsideration and withdrawal of the objections and rejections of record.

CONCLUSION

In light of the above listed remarks, reconsideration of the rejected Claims 1-14 is requested. Based on the arguments presented above, it is respectfully submitted that Claims 1-14 are in condition for allowance.

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Respectfully submitted,
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